contains no mid-term results.

When the detection of the error-containing code is informed by the error-containing code detection signal 22 as in the first embodiment, the contents of the first mid-term result register 81 are not updated, and the subsequent code words are not subjected to error detection.

Step (f-5): the error corrector 6 corrects an error in the code, and transmits the access request signal 17 to the bus control unit 3 to request writing of the error-corrected data to the buffer memory 4.

Step (f-6): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and writes them to the buffer memory 4.

The steps (f-1) through (f-6) are repeated 13 times to complete error correction for one sector, and the error corrector 16 outputs the error completion signal 19 to the system control unit 1.

The above procedure is repeated for 16 sectors to complete the horizontal error correction of one ECC block. When the syndrome is zero in all the code words and the results of the EDCs are zero in all the sectors, or when there is no error in one ECC block, error correction can be completed only by the first-time error correction.

However, in reality, an error-containing code may exist in some cases. Assume that there is an error-containing code on the fifth line (the fifth code word in the horizontal direction) in the second sector as shown in Figure 17. In this case, the mid-term results found in the fifth code word are abandoned, and the contents in the first mid-term result register 81 are not updated. As a result, the mid-term results of the EDCs up to and

including the fourth code word are held in the first mid-term result register 81 until the third-time error correction.

The system control unit 1 enters "18"(13+5) indicating the fifth code word in the second sector as the error-containing code word signal 23 and stores it. The error detecting process is suspended on and after the sixth code word in the second sector, and syndrome calculation is exclusively executed.

The second-time error correction of the second ECC block will be described as follows.

When an error is detected, or when the results of the EDC are other than zero in spite of no error having been detected, the second ECC block is subjected to vertical error correction (the second-time error correction) executed following the horizontal error correction.

Step (f-7): in order to perform the second-time error correction for the second ECC block, the system control unit 1 outputs the DMA command 12 to the DMA control unit 2, so as to provide instructions to transfer data corresponding to one code word in the vertical direction within the second ECC block from the buffer memory 4 only to the syndrome calculator 5. In vertical syndrome calculation, error detection is not executed, but the mid-term results of the first-error correction which are obtained at the second stage and stored in the second mid-term result register 82 are maintained.

Step (f-8): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5.

Step (f-9): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the syndrome data supply signal 15 to the syndrome calculator 5 so as to supply the data read from the buffer memory 4.

Step (f-10): the syndrome calculator 5 calculates the syndrome of each vertical code word in the transferred second ECC block, and outputs the syndrome 16 to the error corrector 6. The syndrome calculator 5 then outputs the error-containing code detection signal 22 to the system control unit 1 when the code word has an error, or when the syndrome 16 is not zero.

Step (f-11): the error corrector 6, after correcting an error in the code, transmits the access request signal 17 to the bus control unit 3 to request writing of the error-corrected data to the buffer memory 4. The error corrector 6 further provides the system control unit 1 with the error correcting position signal 24 indicating the position of the error-corrected data. By using the error correcting position signal 24 and the error-containing code word signal 23 obtained in the first-time error correction, it is determined whether the error correction and the error detection for one ECC block in the third-time error correction should be performed from the beginning or from a halfway point.

Step (f-12): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 61 and writes the data to the buffer memory 4.

The vertical error correction for one ECC block is completed by